Amendments to the Claims

A complete set of the existing claims are set forth below, with the amended claims showing deletions (~~strike through~~) and insertions (underline).

1. (Currently Amended) An apparatus comprising:

a memory cell;

ground control circuitry coupled to the memory cell to programmably control a voltage at a first ground;

~~first circuitry~~ switch circuitry coupled to the memory cell to provide a first voltage to the memory cell during a first period, the first voltage referenced to the first ground; and ~~second circuitry coupled to the memory cell~~ to provide a second voltage to memory cell during a second period, the second voltage referenced to a second ground different from the first ground.

2. (Original) The apparatus of claim 1 wherein the ground control circuitry comprises a plurality of transistors coupled in parallel between the second ground and the first ground.

3. (Original) The apparatus of claim 2 wherein the plurality of transistors coupled in parallel comprise MOSFETs.

4. (Original) The apparatus of claim 2 wherein the plurality of transistors coupled in parallel comprise binary weighted transistors.

5. (Original) The apparatus of claim 1 wherein the first period comprises a period of non-access of the memory cell.

6. (Original) The apparatus of claim 1 wherein the second ground comprises a system ground.

7. (Original) The apparatus of claim 1 further comprising a regulator circuit coupled to the ground control circuitry.

8. (Currently Amended) The apparatus of claim 7 wherein the regulator circuit comprises:

a comparator including a first input coupled to the first ~~circuitry~~ ground[[;]] and a second input coupled to a reference voltage ~~coupled to the comparator~~; and

a counter coupled [[to]] between an output of the comparator and the ground control circuitry.

9. (Original) The apparatus of claim 8 wherein a voltage divider provides the reference voltage.

10.-11. (Cancelled)

12. (Currently Amended) An apparatus comprising:

a memory cell coupled to a supply voltage; and

a ground control circuitry ~~coupled to the memory cell~~ to programmably control a voltage at a ground coupled to the memory cell, the ground control circuitry including a plurality of MOSFET devices that are binary weighted transistors.

13.-25. (Cancelled)

26. (New) The apparatus of claim 1 wherein the switch circuitry includes a first and a second transistor; the first transistor is adapted to couple the first ground to the memory cell during the first period and the second transistor is adapted to decouple the second ground from the memory cell during the first period; and the first transistor is adapted to decouple the first ground from the memory cell during the second period and the second transistor is adapted to couple the second ground to the memory cell during the second period.

27. (New) The apparatus of claim 2 wherein the plurality of transistors are adapted to be configured in response a configuration bit signal to provide a variable resistance between the first ground and the second ground.

28. (New) The apparatus of claim 27 wherein each of the plurality of transistors has a resistance value, with the resistance value being weighted relative to the resistance values of the other transistors.

29. (New) The apparatus of claim 27 wherein the plurality of transistors coupled in parallel comprise n-MOSFETs.